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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/568,312	05/17/2006	Yasuhiko Kasama	80751037	4635
466	7590	02/22/2007	EXAMINER	
YOUNG & THOMPSON			HO, ANTHONY	
745 SOUTH 23RD STREET				
2ND FLOOR			ART UNIT	PAPER NUMBER
ARLINGTON, VA 22202				2815
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE		DELIVERY MODE
3 MONTHS		02/22/2007		PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/568,312	KASAMA ET AL.
	Examiner	Art Unit
	Anthony Ho	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 17 May 2006.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-11 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-11 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 16 February 2006 is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 2/16/2006.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) Notice of Informal Patent Application
- 6) Other: \_\_\_\_\_.

**DETAILED ACTION**

***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Information Disclosure Statement***

The information disclosure statement (IDS) submitted on February 16, 2006 was filed after the mailing date of the instant application on May 17, 2006. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

***Drawings***

Figure 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The disclosure does not mention how one of ordinary skill in the art would be able to form the source and drain regions in the claimed linear device according to the drawings provided by the applicant. In the claimed invention, the source and drain regions are divided and isolated from each other, but there is no details on how one of ordinary skill in the art can obtain such a device. The prior art of record, Solomon et al (US Patent 6,437,422), shows source and drain regions completely surrounded by "linear" semiconductor or isolation material. However, applicant's source and drain regions are physically isolated without surrounding isolation material. The disclosure does not appear to enable such structure.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Solomon et al (US Patent 6,437,422).

In re claim 1, Solomon et al discloses a linear device including a gate electrode, a gate insulating region, a source region, a drain region, and a semiconductor region, characterized in that said semiconductor region is arranged between said source region comprising one or a plurality of source region(s) and said drain region comprising one or a plurality of drain region(s), in a radial direction within a cross section of a device region, so that a part of said gate insulating region is contacted with said semiconductor region (Figure 2).

In re claim 2, Solomon et al discloses gate electrode and gate insulating region are arranged inside or outside source region(s) and drain region(s) (Figure 2).

In re claims 3 and 6, Solomon et al discloses linear device comprises, at a center, one of: a hollow region; an electric conductor region; gate electrode; source region; drain region; another insulating region different from said gate insulating region; and another semiconductor region different from said semiconductor region (Figure 2).

In re claims 4 and 7-8, Solomon et al discloses linear device comprises a plurality of device regions through separation regions there between, respectively, in a longitudinal direction of a linear body constituting said linear device (Figure 2).

In re claims 5 and 9-11, Solomon et al discloses gate electrode, gate insulating region, source region(s), drain region(s), and/or semiconductor region constituting said linear device are formed of an organic semiconductor or electroconductive polymer (column 3 – column 4).

Claims 1-11 are rejected under 35 U.S.C. 102(a) as being anticipated by Kasama et al (JP 2004-193437).

In re claim 1, Kasama et al discloses a linear device including a gate electrode, a gate insulating region, a source region, a drain region, and a semiconductor region, characterized in that said semiconductor region is arranged between said source region comprising one or a plurality of source region(s) and said drain region comprising one or a plurality of drain region(s), in a radial direction within a cross section of a device region, so that a part of said gate insulating region is contacted with said semiconductor region (paragraph 0319; paragraph 0326; paragraph 0331; Drawing 17; Drawing 18; Drawing 19).

In re claim 2, Kasama et al discloses gate electrode and gate insulating region are arranged inside or outside source region(s) and drain region(s) (paragraph 0319; paragraph 0326; paragraph 0331; Drawing 17; Drawing 18; Drawing 19).

In re claims 3 and 6, Kasama et al discloses linear device comprises, at a center, one of: a hollow region; an electric conductor region; gate electrode; source region; drain region; another insulating region different from said gate insulating region; and another semiconductor region different from said semiconductor region (paragraph 0319; paragraph 0326; paragraph 0331; Drawing 17; Drawing 18; Drawing 19).

In re claims 4 and 7-8, Kasama et al discloses linear device comprises a plurality of device regions through separation regions there between, respectively, in a longitudinal direction of a linear body constituting said linear device (paragraph 0319; paragraph 0326; paragraph 0331; Drawing 17; Drawing 18; Drawing 19).

In re claims 5 and 9-11, Kasama et al discloses gate electrode, gate insulating region, source region(s), drain region(s), and/or semiconductor region constituting said linear device are formed of an organic semiconductor or electroconductive polymer (entire document).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Ho whose telephone number is 571-270-1432. The examiner can normally be reached on M-Th: 8:30AM-7:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH  
February 16, 2007



EROME JACKSON  
MARY EXAMINER